REMARKS

This paper is being provided in response to the Office Action dated September 2, 2003, for the above-referenced application. In this response, Applicant has amended the specification and amended claims in order to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the specification do not add new matter and that the changes to the claims are fully supported by the originally filed application.

Applicant has amended the specification for purposes of clarification to correct an error concerning the identification of elements V43 and V45 in Figure 4. These elements are shown in Figure 4 as NOR gates; however, they are identified in the specification on pages 21 and 22 as NAND gates. Applicant has corrected the specification to identify these elements as NOR gates so as to bring the specification in conformance with the originally-filed and drawing. Applicant respectfully submits that no new matter is added by this amendment.

Applicant thanks the Examiner for allowing claims 15 and 22-24 and for the indication of allowable subject matter in claim 20. Applicant has made a minor typographical correction to claim 15 and has rewritten claim 20 into independent form to incorporate the features of the base claim and any intervening claims. Applicant respectfully submits that claim 20 is in condition for allowance.

The rejection of claims 25 under 35 U.S.C. 112, first paragraph, is hereby traversed in view of the amendments to the specification contained herein. The Office Action states that the feature of claim 25 of "a NOR gate receiving the logic signal and the output signal" is not

supported in the specification or drawings as originally filed. As noted above, Applicant respectfully submits that elements V43 and V45 are shown as NOR gates in originally-filed Figure 4 but incorrectly identified as NAND gates in the specification. Applicant has amended the specification to correct this error and bring the specification and drawing into conformance with one another. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 19, 21, 27 and 28 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,055,713 to Watanabe et al. (hereinafter "Watanabe") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 19, as amended herein, recites a delay circuit. The circuit includes first and second nodes and first and second inverters. The first inverter receives a logic signal and its output is coupled to the first node. The input of the second inverter is coupled to the first node and the output is coupled to the second node. A first capacitor is coupled between the first node and a first power source line, the first capacitor being a first transistor of a first channel type. The second capacitor is coupled between the second node and a second power source line different from the first power source line, the second capacitor being a second transistor of a second channel type different from the first channel type. Further, when the logic signal is fixed at a low level during a standby state, one of the first capacitor and the second capacitor is set to an off-state in response to a chip select signal controlling the standby state, and the other of the first capacitor and the second capacitor is set to an off-state in response to the chip select signal

that is negated. Claim 21 depends on independent claim 19 and recites additional patentable features thereto.

Independent claim 27, as amended herein, recites a delay circuit receiving a logic signal having a first logical level and a second logical level. An inverter chain is included including a plurality of inverters and at least one first capacitor, the inverter chain receiving a logic signal. The first capacitor includes a MOS transistor of a first channel type. The capacitor is operated to increase and decrease capacitance based on changes in the logical levels of the logic signal and whereby a first delay signal and a second delay signal are generated, the second delay time being shorter than the first delay time. A logical gate receives the output of the inverter chain and the logic signal so that the logical gate outputs its output signal in response to the first delay signal when the logic signal changes from the first logical level to the second logical level. Further, when the logic signal is fixed at a low level during a standby state, said first capacitor is set to an off-state in response to a chip select signal controlling said standby state. Claim 28 depends on independent claim 27 and recites additional patentable features thereto.

The Watanabe reference discloses an output circuit of an integrated circuit including first and second MOS transistors and a drive and control circuit. In Figure 5, Watanabe discloses two inverters (I2 and I3), two capacitors (C1 and C2) and power source lines (VSS and VCC) with an output directed to a logic gate (a NAND gate-NA1).

Applicant's independent claims, as amended herein, recite at least the feature that when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an

off-state in response to a chip select signal controlling the standby state. In structures based on MOS capacitors or inverters comprising MOS transistors, generation of leak current during the standby state is suppressed and thereby source-voltage dependency of the delay time is contained and power consumption is effectively controlled during the standby state. (See Figure 10 and page 32, line 2 to page 33, line 4 of the present application).

Applicant respectfully submits that Watanabe does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Watanabe does not disclose the circuit configuration as claimed by Applicant including capacitors that comprise MOS transistors and wherein when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an off-state in response to a chip select signal controlling the standby state. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claim 26 under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of U.S. Patent No. 4,803,665 to Kasa (hereinafter "Kasa") is hereby traversed and reconsideration is respectfully requested.

Independent claim 26, as amended herein, recites a delay circuit including first and second nodes and first and second inverters. An input of the first inverter receives a logic signal and the output is coupled to the first node. An input of the second inverter is coupled to the first node and the output is coupled to the second node. A first capacitor of a first MOS type is coupled between the first node and a first power source line. A second capacitor of a second MOS type is coupled between the second node and a second power source line. An AND gate

receives the logic signal and a signal on the second node. Further, when the logic signal is fixed at a low level during a standby state, one of said first capacitor and said second capacitor is set to an off-state in response to a chip select signal controlling said standby state, and the other of said first capacitor and said second capacitor is set to an off-state in response to said chip select signal that is negated.

The Kasa reference discloses a signal transition detection circuit including a delay circuit and a logic circuit. Kasa is cited by the Office Action as disclosing an AND gate receiving a logic signal and a signal on a second node.

Applicant respectfully submits that Kasa fails to overcome the above-noted deficiencies of the Watanabe reference with respect to Applicant's claims. Specifically, Applicant respectfully submits that neither Watanabe nor Kasa, taken alone or in any combination, teach or fairly suggest the feature that when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an off-state in response to a chip select signal controlling the standby state. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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